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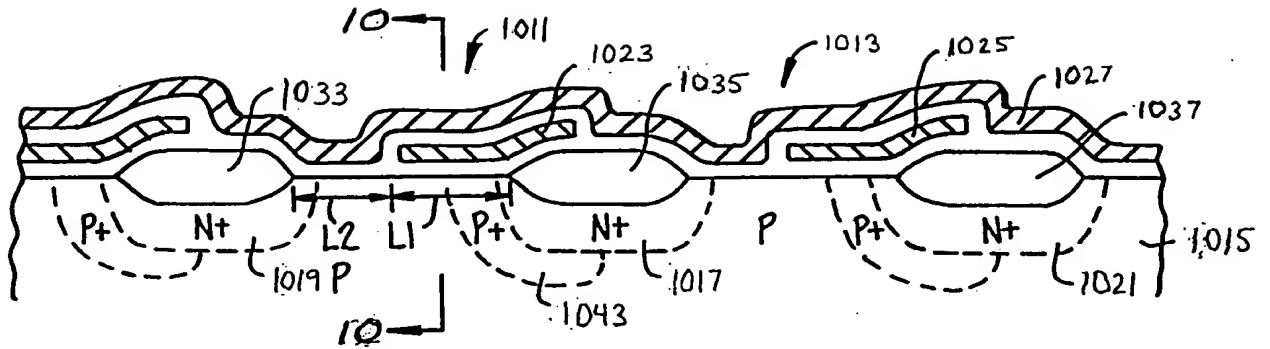


FIG. 9

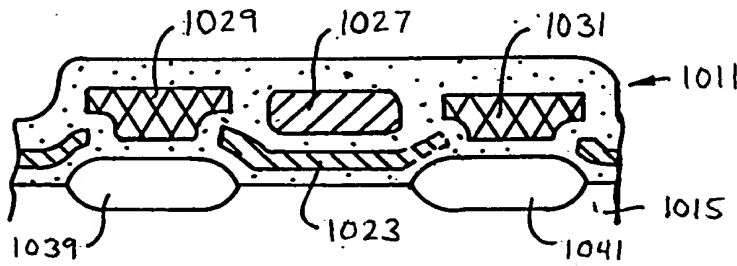


FIG. 10

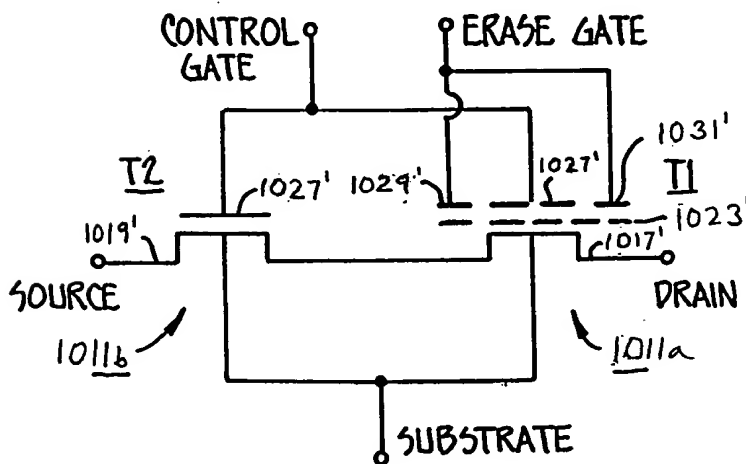
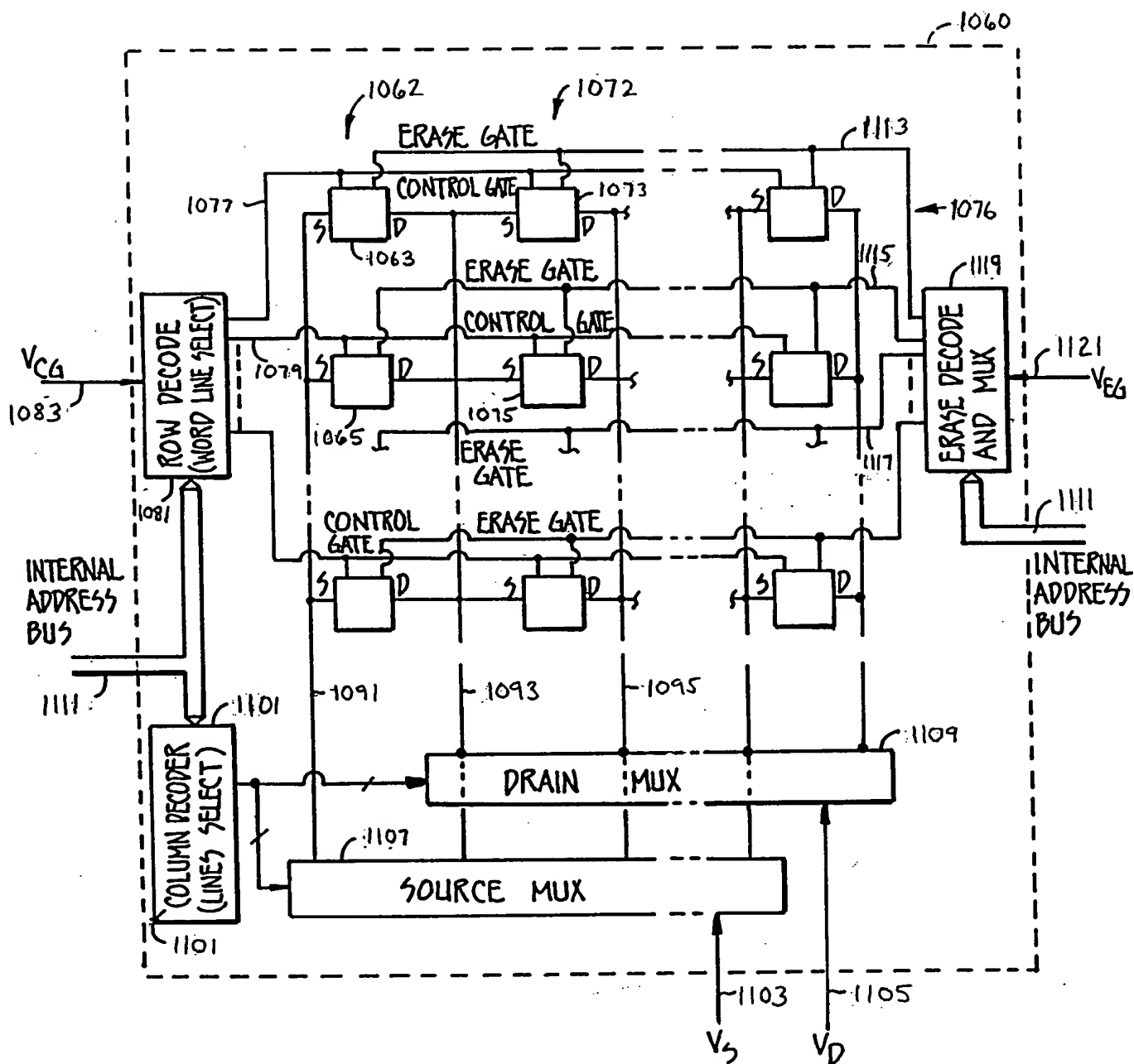


FIG. 11



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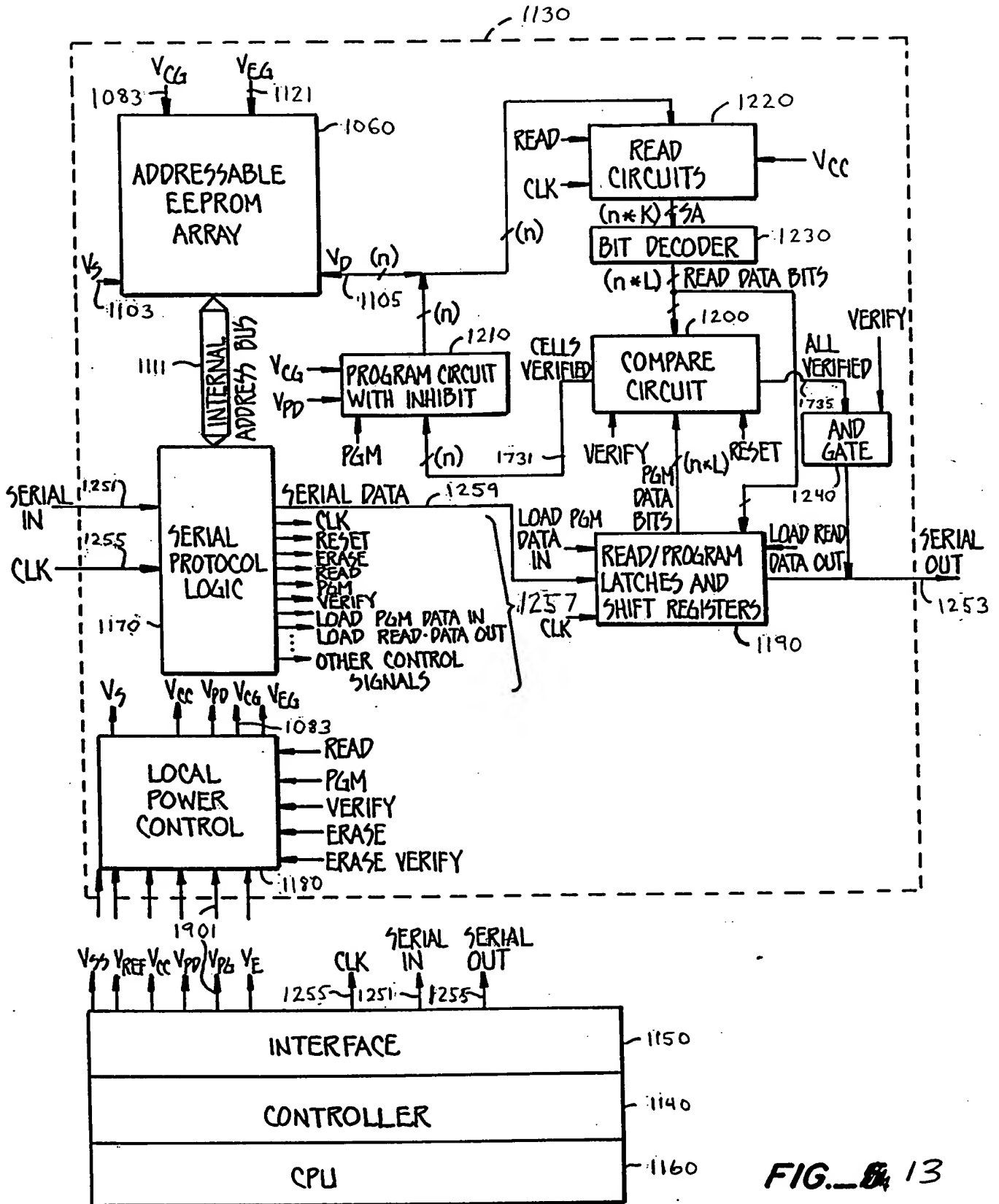


FIG. 13

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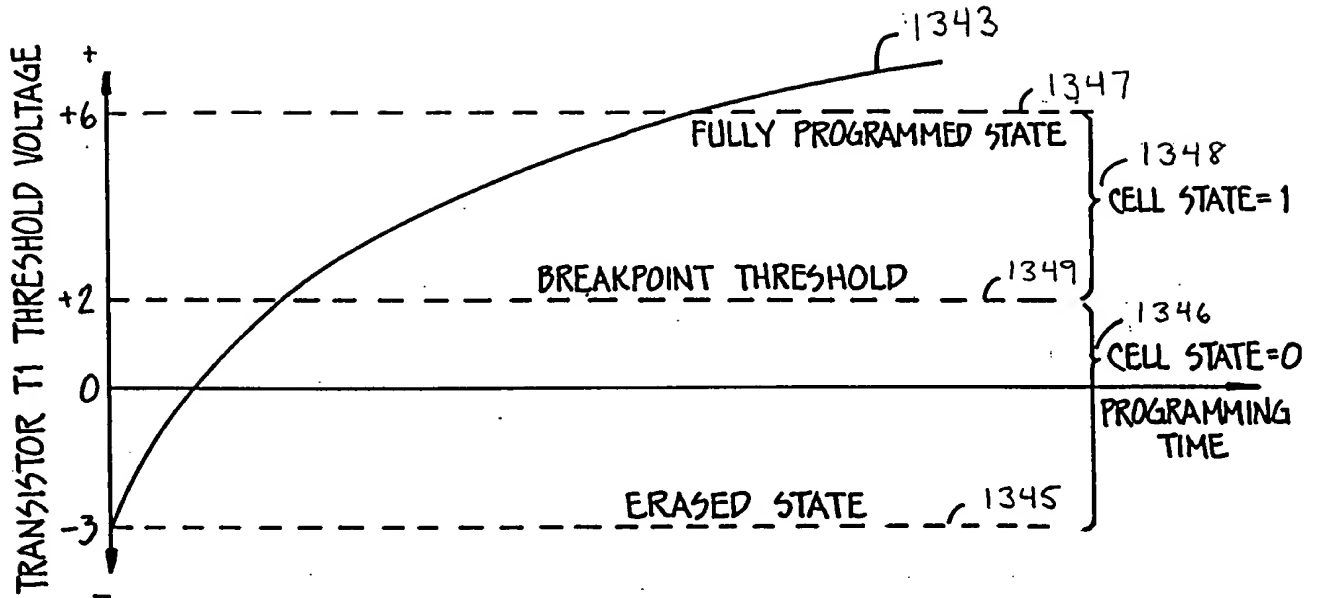


FIG. 14.

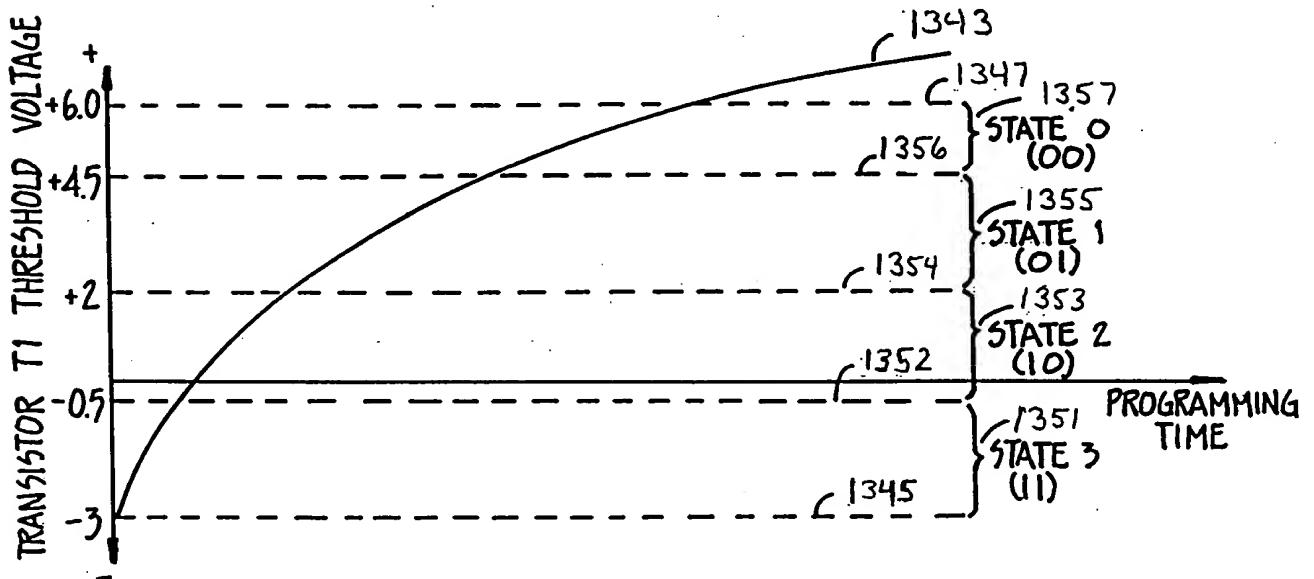


FIG. 15A

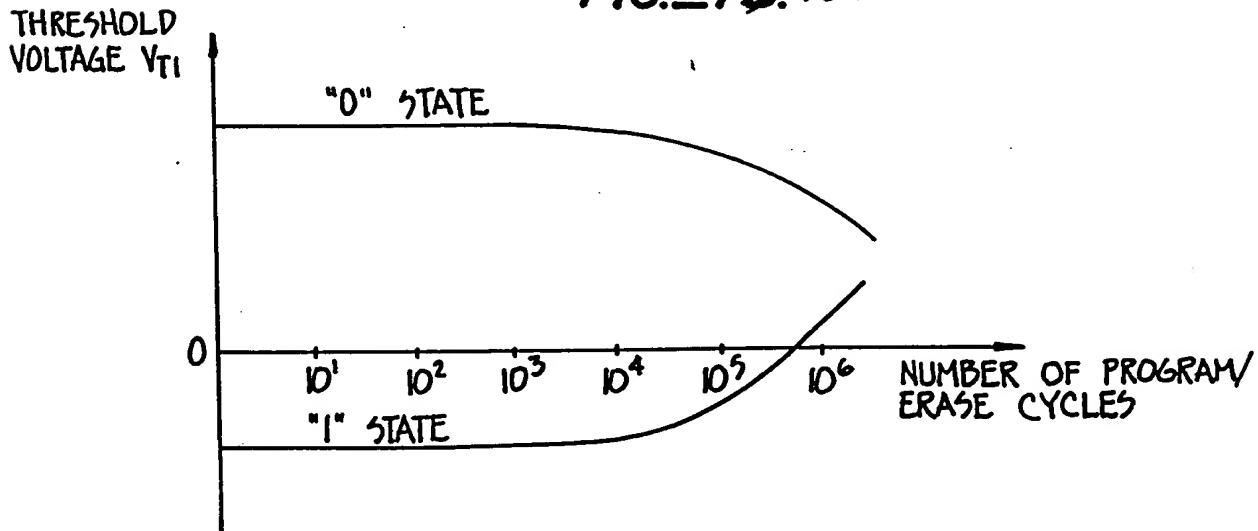
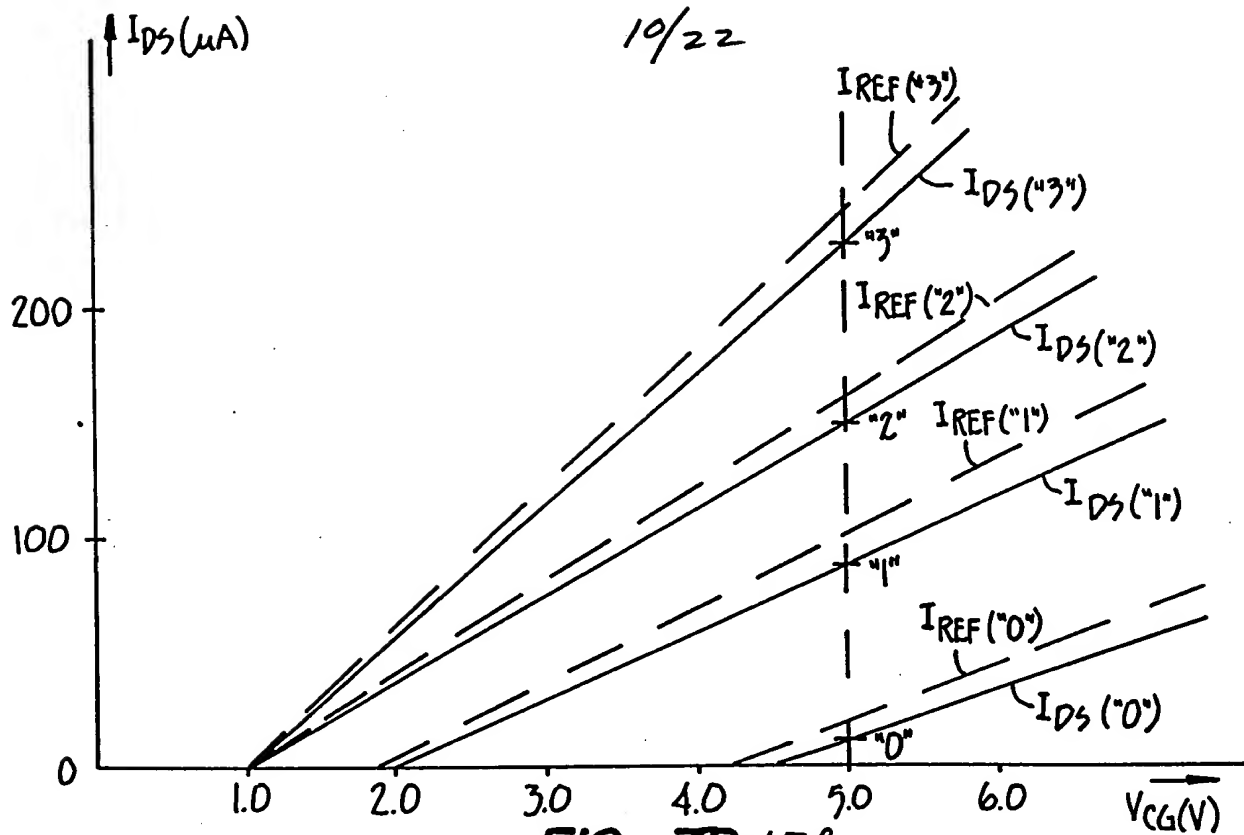
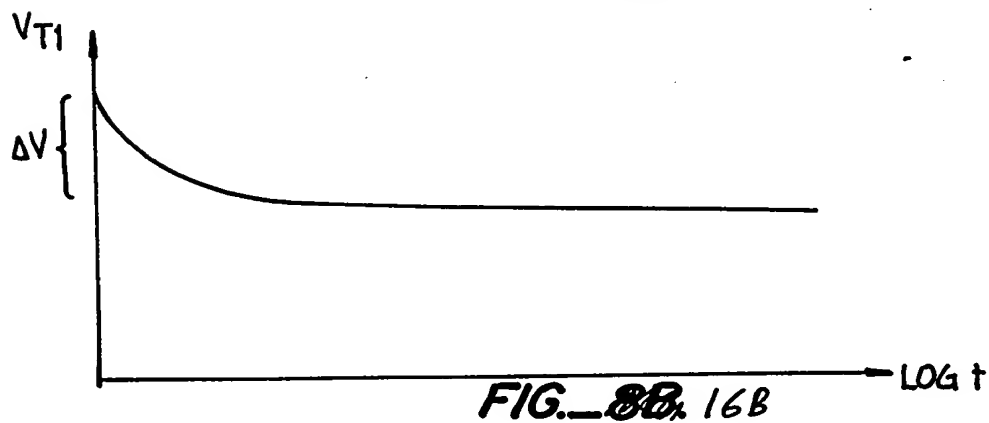


FIG. 16A



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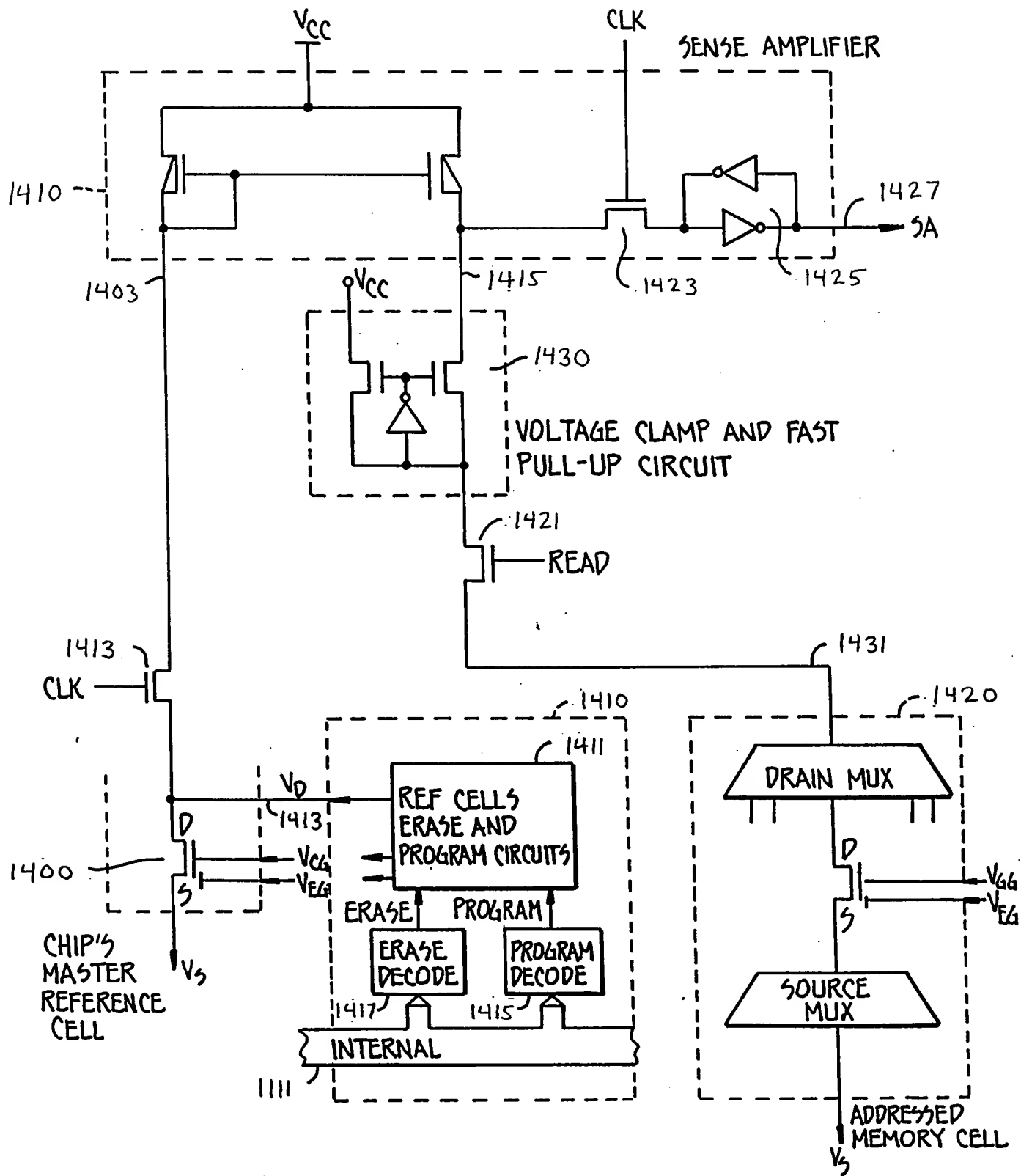


FIG. 17A

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36607-2788760

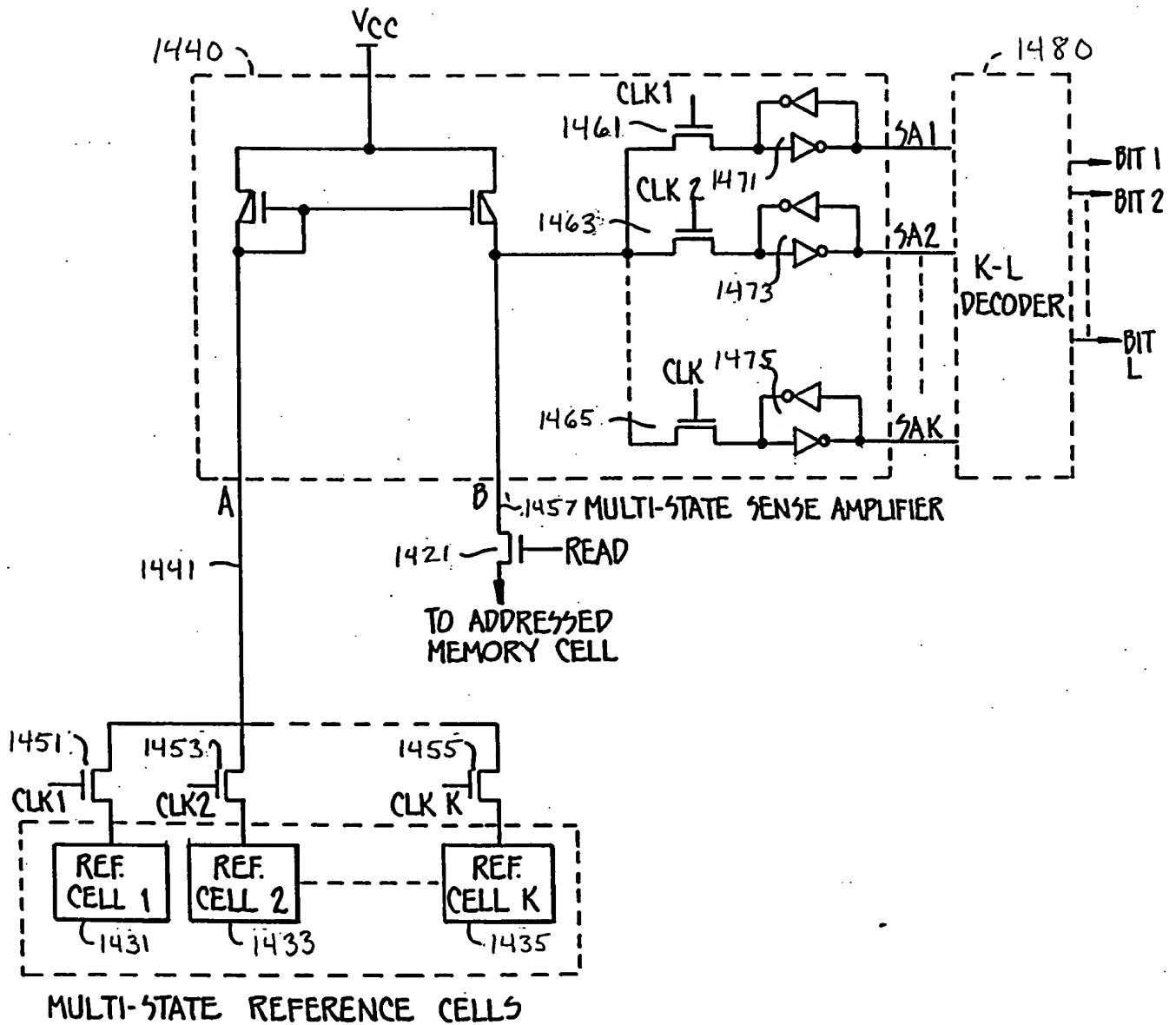


FIG. 17B

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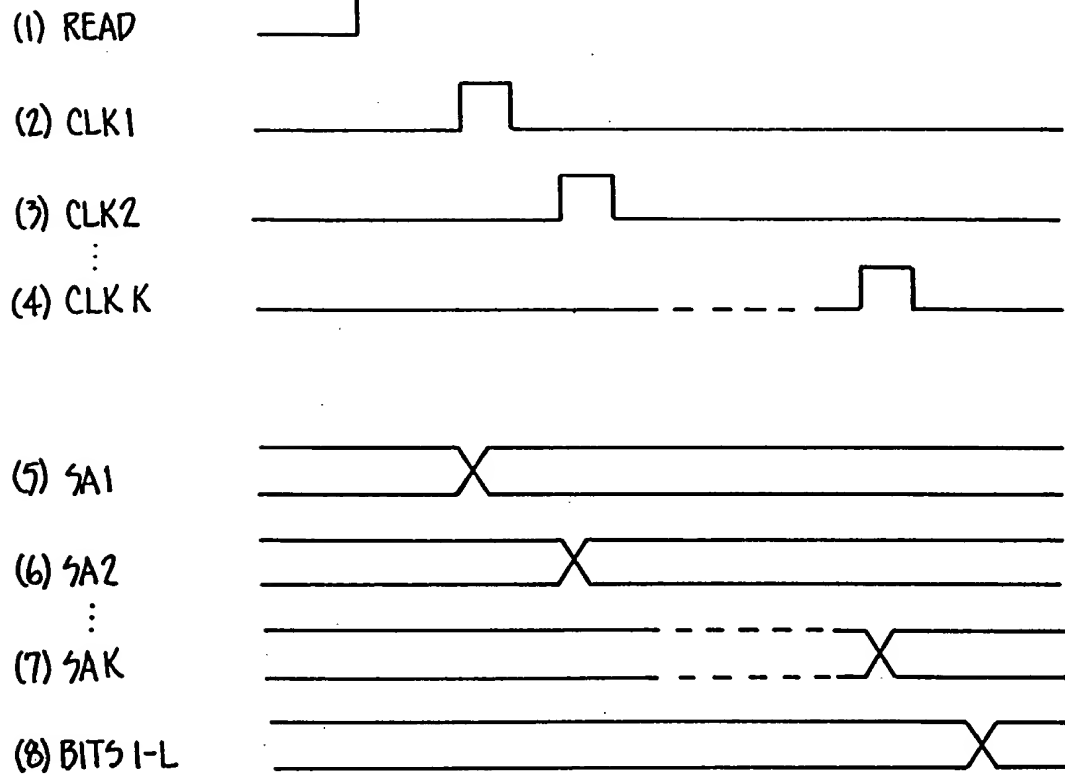


FIG. ~~10~~ 17C

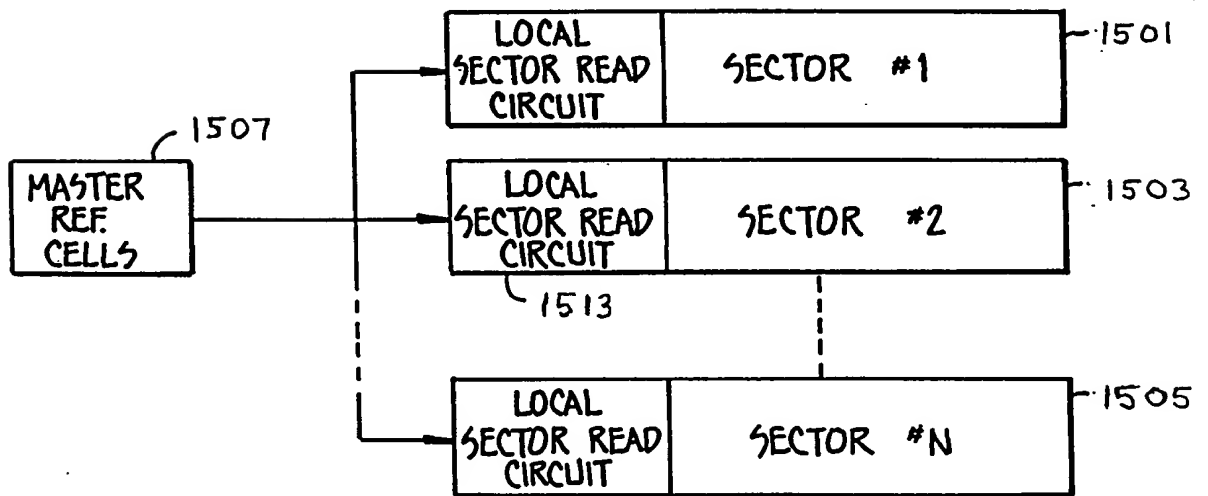
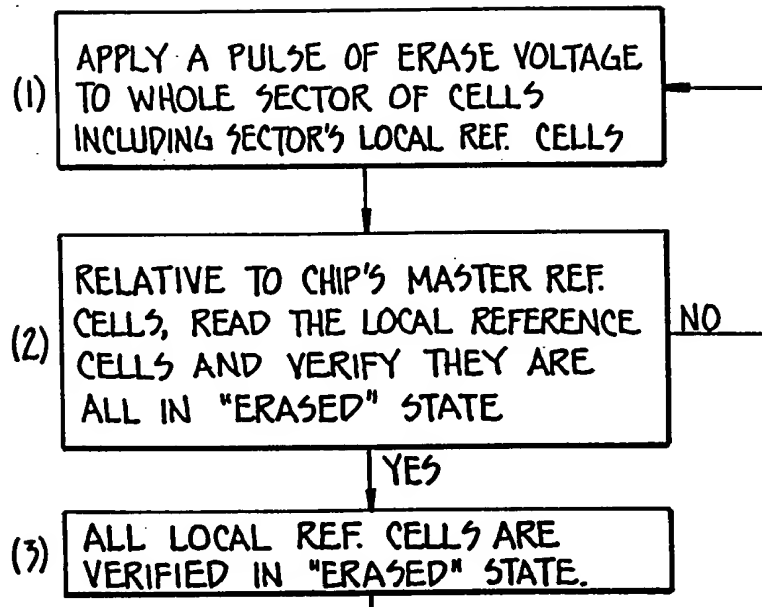


FIG. ~~10~~ 18

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SECTOR LOCAL
REF. CELLS ERASE
AND VERIFY
ALGORITHM



SECTOR'S LOCAL
REF. CELLS
PROGRAM AND
VERIFY ALGORITHM

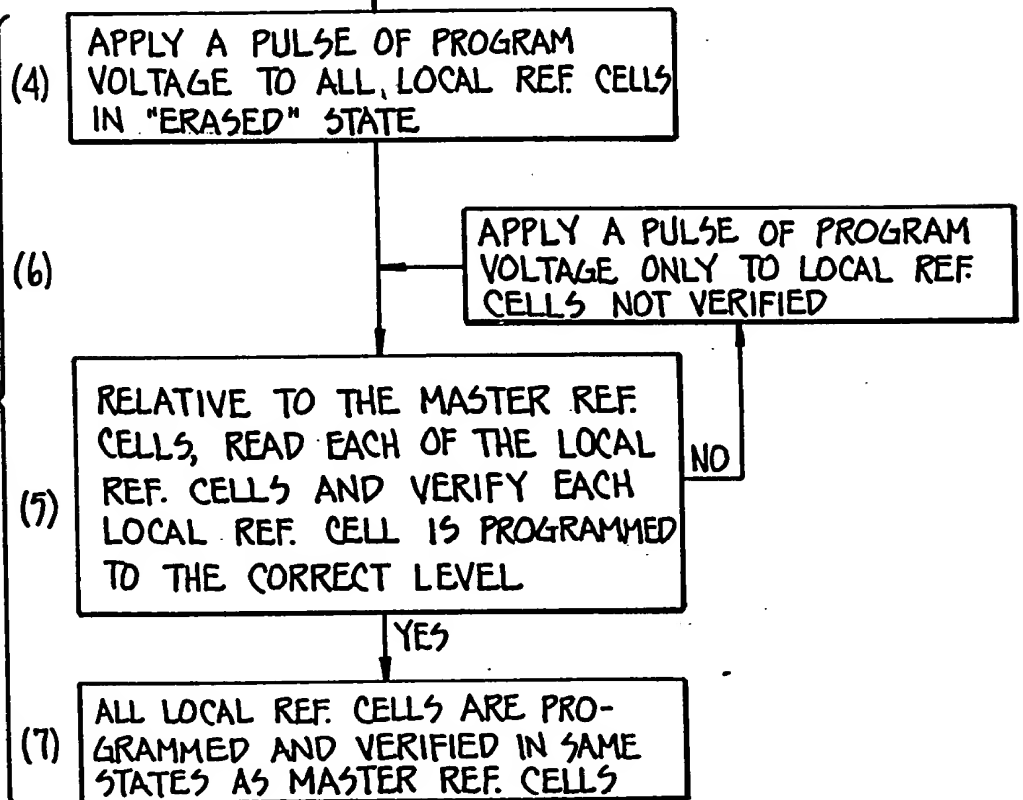


FIG. # 19

094841-1098

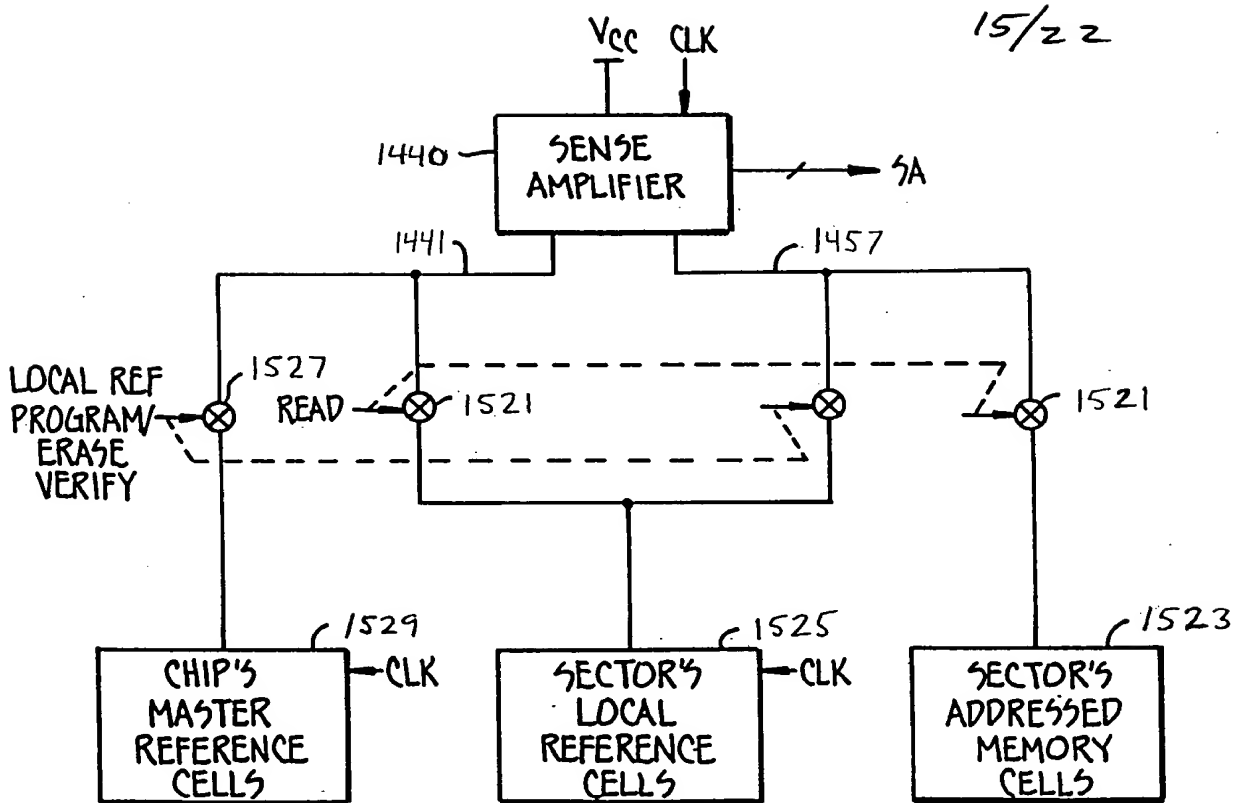


FIG. 20A

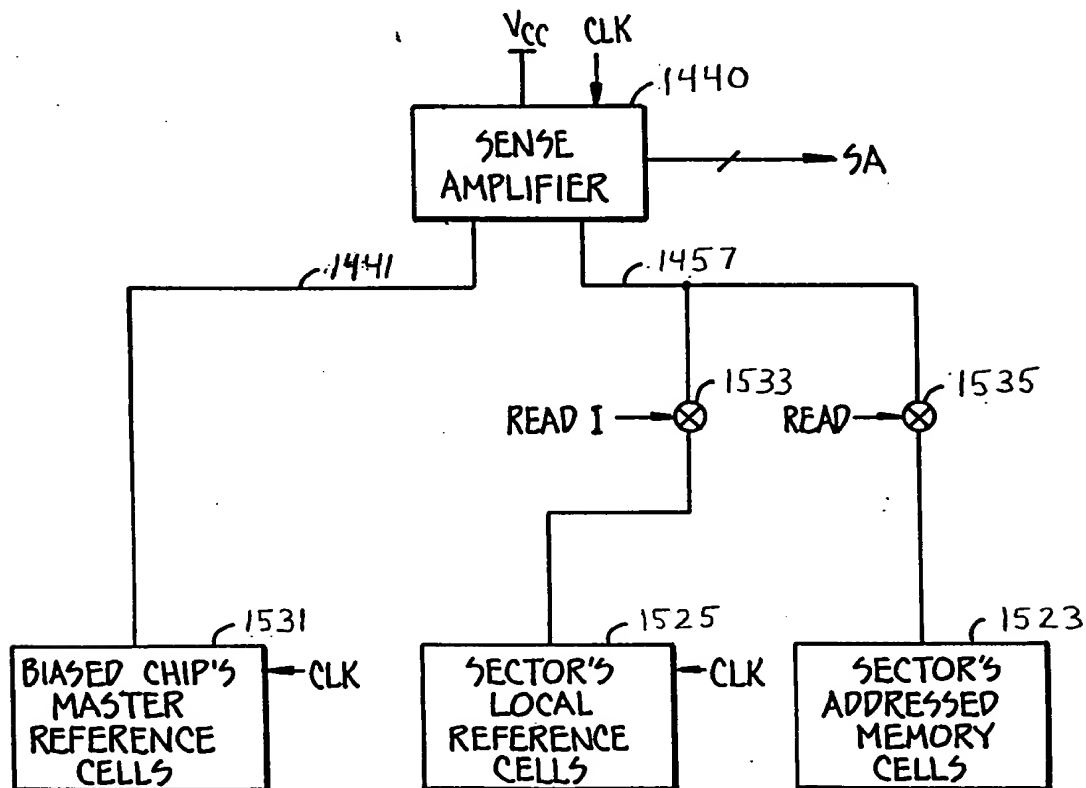


FIG. 21A

[illegible]

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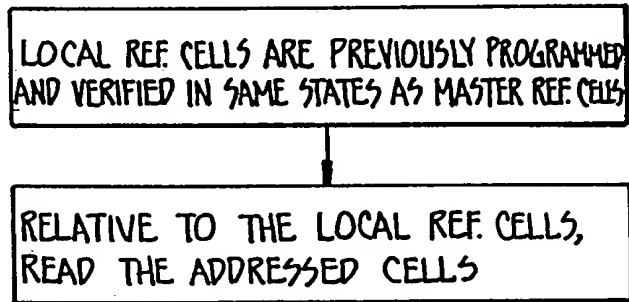


FIG. ~~12B~~, 20B

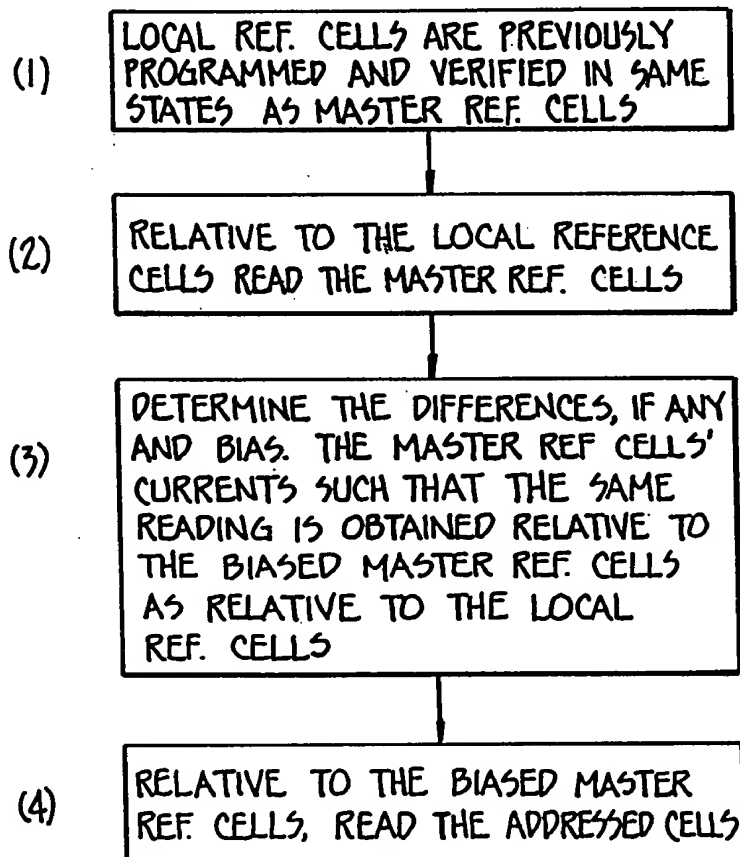
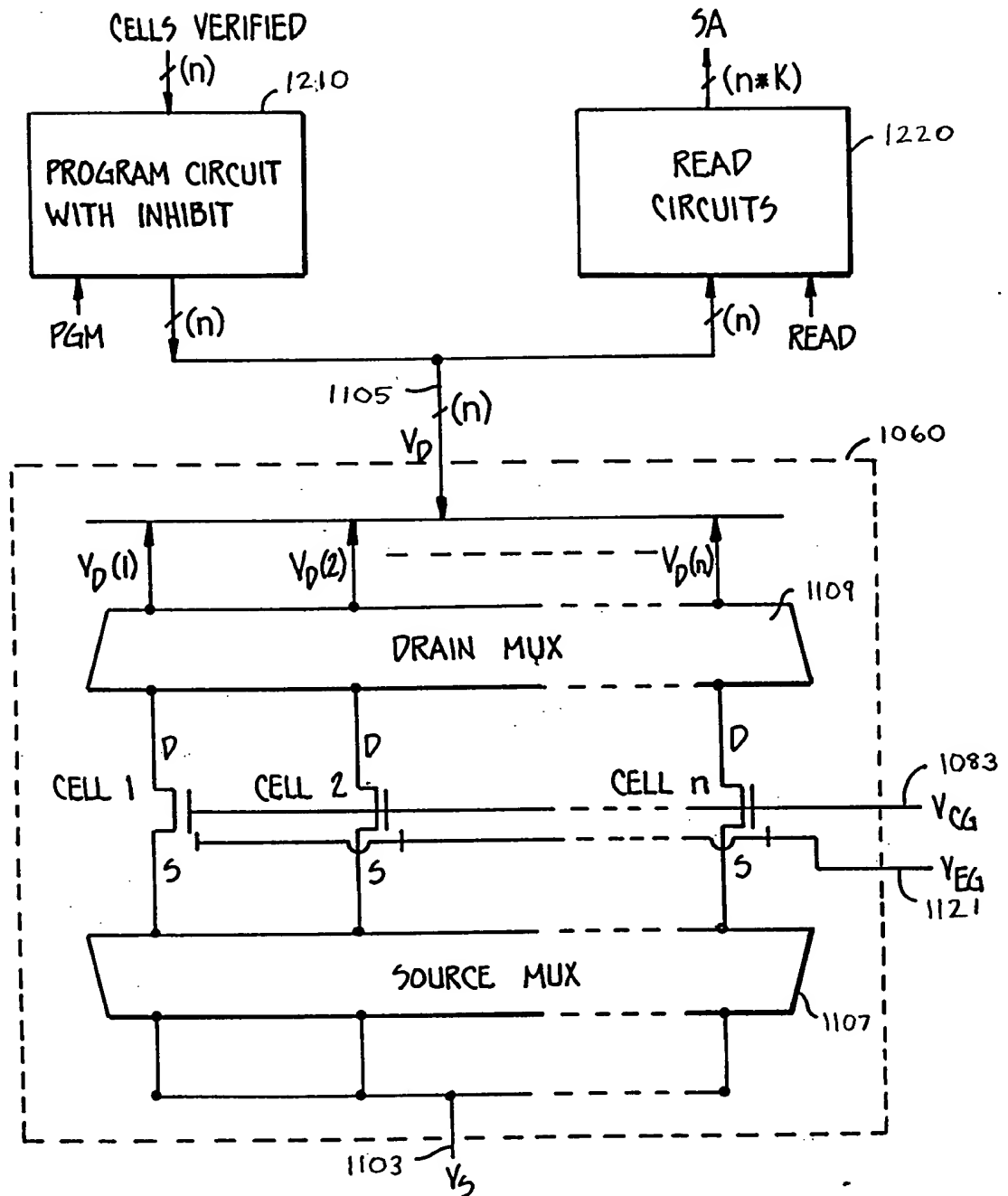


FIG. ~~13D~~, 21D

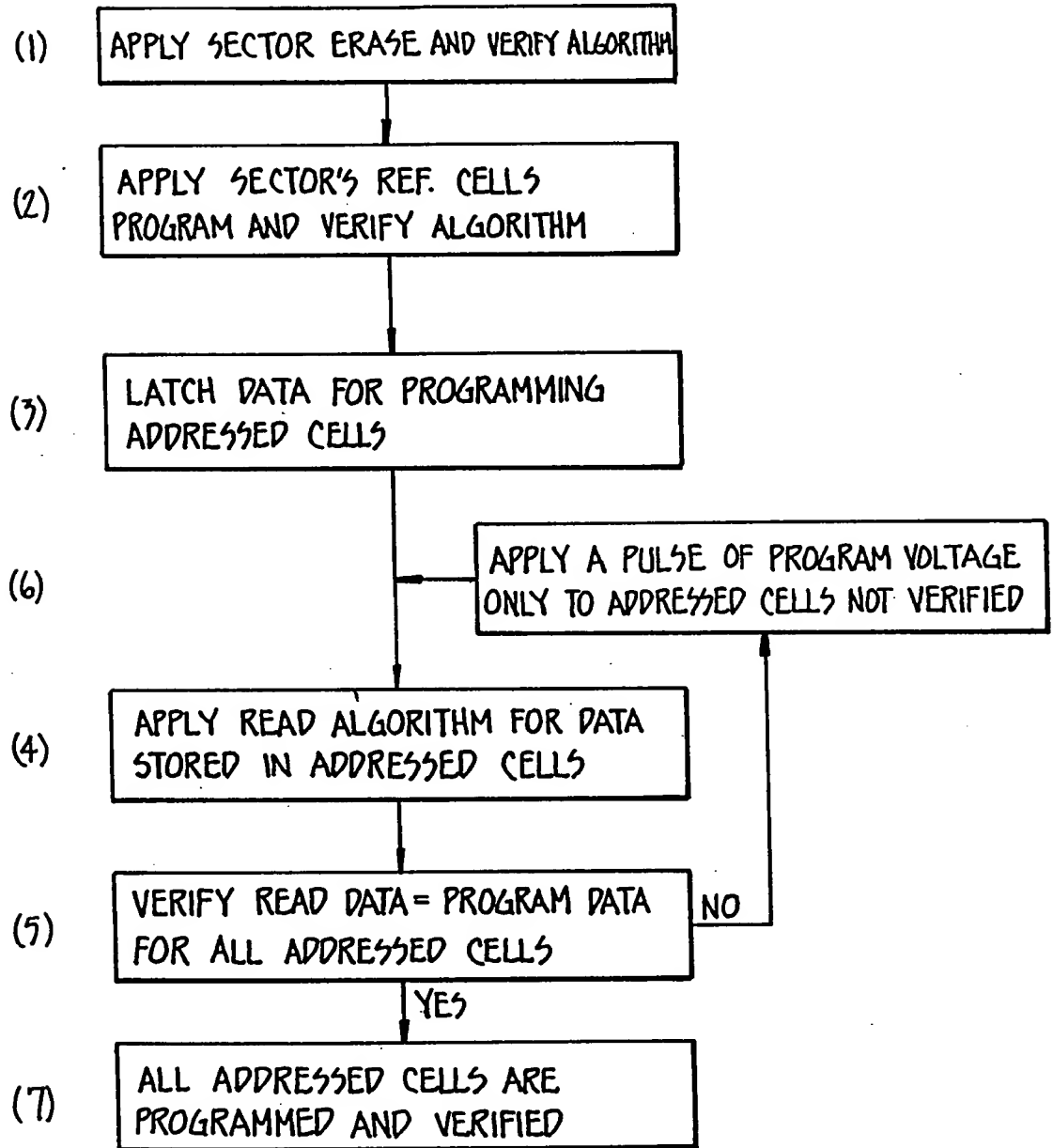
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READ/PROGRAM DATA PATHS FOR n CELLS IN PARALLEL

FIG. 22.

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PROGRAM ALGORITHM

FIG. 23

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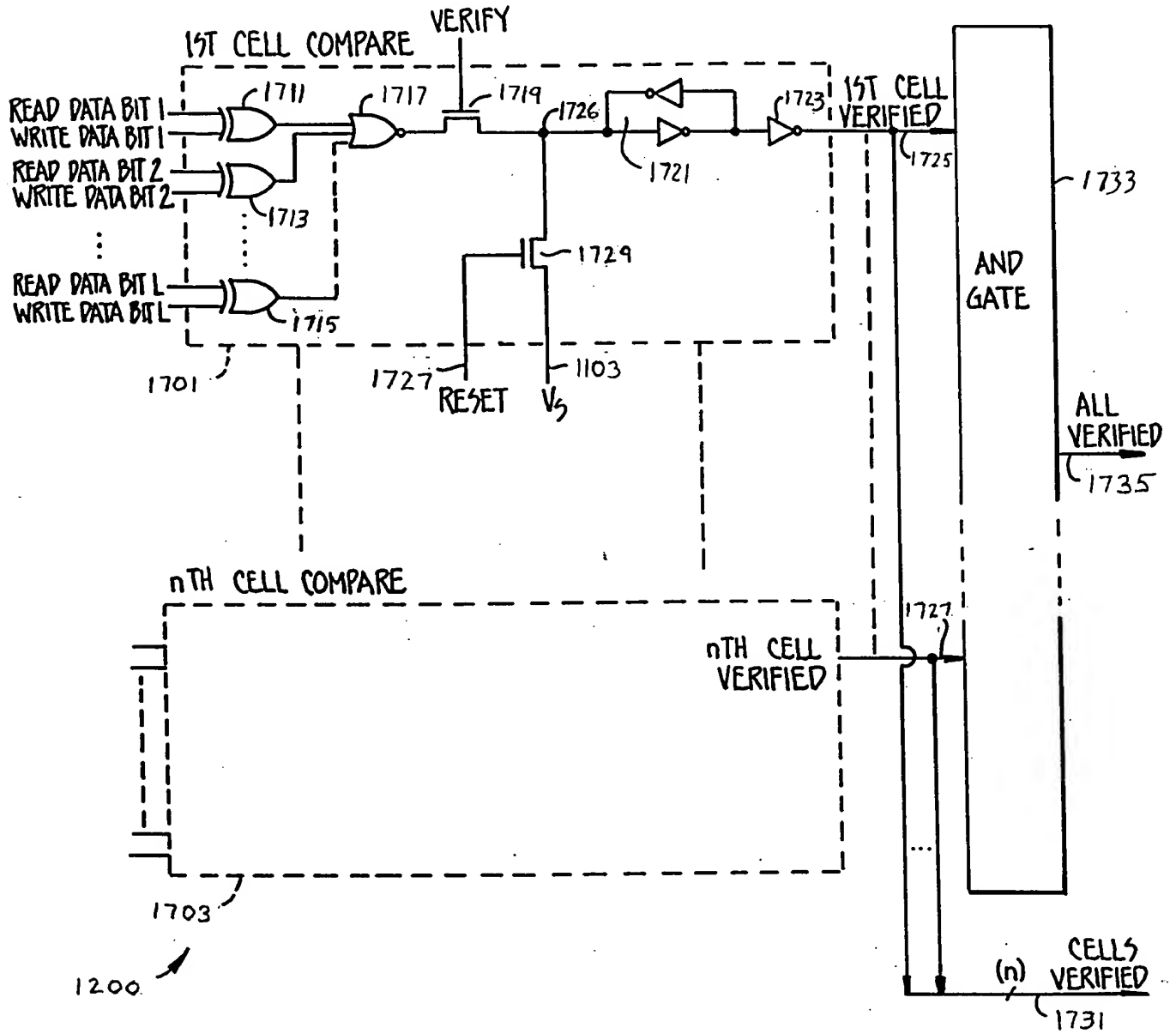


FIG. 16. 24

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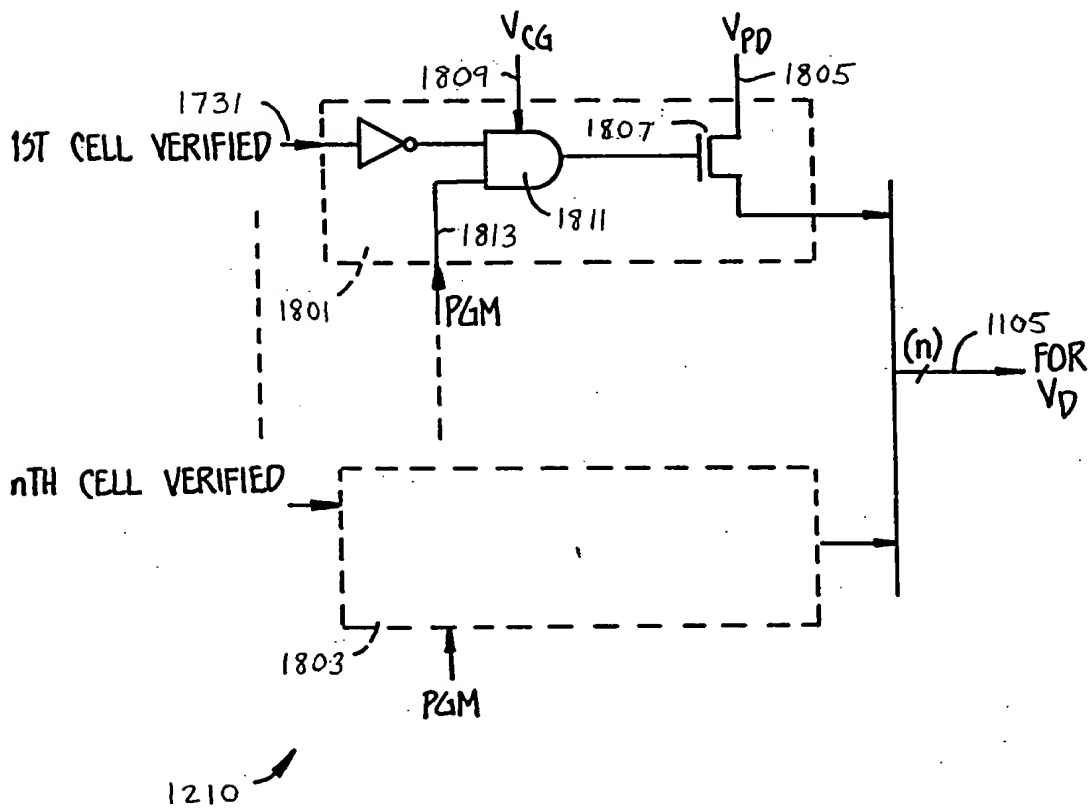


FIG. 25

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	SELECTED CONTROL GATE V_{CC}	DRAIN V_D	SOURCE V_S	ERASE GATE V_{EG}
READ	V_{PG}	V_{REF}	V_{SS}	V_E
PROGRAM	V_{PG}	V_{PD}	V_{SS}	V_E
PROGRAM VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE	V_{PG}	V_{REF}	V_{SS}	V_E
ERASE VERIFY	V_{PG}	V_{REF}	V_{SS}	V_E

~~TABLE 1~~ FIG. 26

(typical values)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
V_{PG}	V_{CC}	12V	$V_{CC} + \delta V$	V_{CC}	$V_{CC} - \delta V$
V_{CC}	5V	5V	5V	5V	5V
V_{PD}	V_{SS}	8V	8V	V_{SS}	V_{SS}
V_E	V_{SS}	V_{SS}	V_{SS}	20V	V_{SS}
unselected control gate	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
unselected bit line	V_{REF}	V_{REF}	V_{REF}	V_{REF}	V_{REF}

$V_{SS}=0V$, $V_{REF}=1.5V$, $\delta V=0.5V - 1V$

~~TABLE 2~~ FIG. 27

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